SECTION I—CLAIMS

Amendment to the Claims:

This listing of the claims will replace all prior versions and listings of claims in the application. Claims 1-12, 15, and 20-30 are herein canceled without prejudice. Please enter new claims 31-60.

Listing of Claims:

1-12. (Canceled)

13. (Currently amended) A method, comprising:

enabling a plurality of network processors to access a first shared memory store and a second shared memory store[[s]]; and

~~employing a first portion of the first shared memory store as a memory store;~~

employing a ~~second~~ portion of the first shared memory store as a memory cache for the second shared memory store[[.]];

each network processor having a cache management component retrieving data from the memory cache, and a content addressable memory component performing content based searches of the first and second shared memory stores.

14. (Currently amended) The method of claim 13, wherein the first shared memory store and the second shared memory store ~~comprises static random access memory (SRAM)~~ are selected from a group of shared memory stores consisting of dynamic random access memory (DRAM), Rambus dynamic random access memory (RDRAM), static random access memory (SRAM), reduced latency dynamic random access memory (RLDRAM), double data rate dynamic random access memory (DDR DRAM), double data rate two dynamic random access memory (DDR-2),

double data rate three dynamic random access memory (DDR-3), and fast cycle dynamic random access memory (FCDRAM).

15. (Canceled).

16. (Currently amended) The method of claim 13, further comprising:

configuring the memory cache as a cache array including a plurality of cache lines; and

maintaining a local address-to-cache line map in the cache management component of each network processor ~~on each of the plurality of network processors~~ in which cache lines associated with ~~that~~ the respective network processor are mapped to corresponding memory addresses in an address space for the second shared memory store.

17. (Currently amended) The method of claim 16, further comprising:

broadcasting a cache line access request to the plurality of network processors in response to a memory access request from a requesting network processor[[s]]; and

performing a cache line lookup in the local address-to-cache line map of each network processor to determine which, if any, network processors own[[s]] a cache line of the plurality of cache lines corresponding to the memory access request.

18. (Currently amended) The method of claim 17, further comprising:

accessing the cache line to service the memory access request if it is determined that one of the network processors own[[s]] the cache line; and

releasing ownership of the cache line by updating ~~modifying entries in~~ the local address-to-cache line map[[s]] for ~~each of~~ the network processor that owned the cache line and assigning ownership of the cache line by updating the local address-to-cache line map for the requesting network processor ~~to reassign ownership of the cache line to the requesting network processor~~.

19. (Currently amended) The method of claim 17, further comprising:

~~accessing memory~~ retrieving data from the second shared memory store if it is determined that none of the network processors own[[s]] the cache line;

selecting a cache line in the memory cache to replace;

copying data ~~corresponding to data contained in the memory in~~ from the second shared memory store ~~that is accessed to~~ into the cache line selected for replacement ~~to be replaced~~; and

~~modifying~~ updating the local address-to-cache line map of the requesting network processor to assign ownership of the replaced cache line ~~that is replaced~~ to the requesting network processor.

20-30. (Canceled).

31. (New) A computing apparatus comprising:

an internal interconnect;

a first memory store, coupled with the internal interconnect via a first memory controller;

a second memory store, coupled with the internal interconnect via a second memory controller;

a cache management component coupled with the internal interconnect to effectuate a memory cache in a portion of the first memory store corresponding to data in the second memory store; and

a content addressable memory component to perform content based searching of the first and second memory stores.

32. (New) The computing apparatus of claim 31 wherein the first and second memory stores are selected from a group of memory stores consisting of dynamic random access memory (DRAM), Rambus dynamic random access memory (RDRAM), static random access memory (SRAM), reduced latency dynamic random access memory (RLDRAM), double data rate dynamic random access memory (DDR DRAM), double data rate two dynamic random access

memory (DDR-2), double data rate three dynamic random access memory (DDR-3), and fast cycle dynamic random access memory (FCDRAM).

33. (New) The computing apparatus of claim 31, wherein the first memory store comprises a static random access memory store and the second memory store comprises a Rambus dynamic random access memory store.

34. (New) The computing apparatus of claim 31, wherein the content addressable memory component is implemented in software or firmware.

35. (New) The computing apparatus of claim 31, wherein the content addressable memory component is implemented in hardware.

36. (New) The computing apparatus of claim 31, wherein the content addressable memory component is integrated with the cache management component in hardware.

37. (New) The computing apparatus of claim 31, wherein first memory store comprises a static random access memory store integrated onto the network processor.

38. (New) The computing apparatus of claim 31, wherein the first memory store further comprises:

a plurality of non-contiguous memory cache regions; and

a plurality of non-contiguous general use regions.

39. (New) The computing apparatus of claim 31, wherein the cache management component is configured to maintain a hardware-based cache tag array.

40. (New) The computing apparatus of claim 31, wherein the cache management component further comprises:

a first computer instruction to support concurrent execution of a plurality of threads;

a second computer instruction to maintain an address tag array for each of said plurality of threads; and

a third computer instruction to maintain a data cache for each of said plurality of threads.

41. (New) The computing apparatus of claim 31, wherein the cache management component, the internal interconnect, and the content addressable memory component comprise a network processor.

42. (New) The computing apparatus of claim 41, further comprising:

a third memory store, coupled with the internal interconnect via an interface controller, wherein the interface controller is configured to receive memory access requests.

43. (New) The computing apparatus of claim 42, wherein the interface controller comprises a front side bus interface controller integrated on the network processor.

44. (New) The computing apparatus of claim 43, wherein the network processor further comprises a general-purpose processor component configured to store data on the second memory store.

45. (New) The computing apparatus of claim 31, further comprising:

a fourth interface coupled between the first memory controller and the cache management component to transmit memory access requests.

46. (New) A network processor, comprising:

an internal interconnect;

a first memory controller coupled with the internal interconnect to access a first off-chip memory store;

a second memory controller coupled with the internal interconnect to access a second off-chip memory store;

a first portion of the first off-chip memory store configured as a memory cache for the second off-chip memory store;

a cache management component coupled with the internal interconnect to retrieve data in the memory cache;

a content addressable memory component to perform content based searching of the first and second off-chip memory stores; and

a front side bus controller coupled with the internal interconnect to receive memory requests.

47. (New) The network processor of claim 46, wherein the first off-chip memory store comprises static random access memory (SRAM).

48. (New) The network processor of claim 46, wherein the second off-chip memory store is selected from a group of memory stores consisting of dynamic random access memory (DRAM), Rambus dynamic random access memory (RDRAM), static random access memory (SRAM), reduced latency dynamic random access memory (RLDRAM), double data rate dynamic random access memory (DDR DRAM), double data rate two dynamic random access memory (DDR-2), double data rate three dynamic random access memory (DDR-3), and fast cycle dynamic random access memory (FCDRAM).

49. (New) The network processor of claim 46, further comprising:

a third memory controller coupled with the internal interconnect to access a third off-chip memory store, wherein the cache management component is configured to manage the memory cache corresponding to a memory address space for the third memory store.

50. (New) The network processor of claim 49, wherein the third off-chip memory store is accessed via an off-chip front side bus and the off-chip front side bus is coupled with the front side bus controller.

51. (New) The network processor of claim 49, wherein the third off-chip memory store is selected from a group of memory stores consisting of dynamic random access memory (DRAM), Rambus dynamic random access memory (RDRAM), static random access memory (SRAM), reduced latency dynamic random access memory (RLDRAM), double data rate dynamic random access memory (DDR DRAM), double data rate two dynamic random access memory (DDR-2), double data rate three dynamic random access memory (DDR-3), and fast cycle dynamic random access memory (FCDRAM).

52. (New) The network processor of claim 46, further comprising:

a communication channel linking the first memory controller to the cache management component to transmit memory access requests.

53. (New) The network processor of claim 46, wherein the cache management component is configured to maintain a hardware-based cache tag array.

54. (New) The network processor of claim 46, wherein the cache management component is configured to manage a cache tag array in a second portion of the first off-chip memory store.

55. (New) A system, comprising:

a first memory store, with a first interface;

a second memory store with a second interface; and

a network processor comprising:

an internal interconnect;

a first memory controller coupled with the internal interconnect to access the first memory store;

a second memory controller coupled with the internal interconnect to access the second memory store;

a cache management component coupled with the internal interconnect to effectuate a memory cache in a portion of the first memory store corresponding to data in the second memory store;

a content addressable memory component to perform content based searching of the first and second memory stores; and

an interface controller coupled with the internal interconnect to receive memory requests via the second interface.

56. (New) The system of claim 55, wherein the first and second memory stores are selected from a group of memory stores consisting of dynamic random access memory (DRAM), Rambus dynamic random access memory (RDRAM), static random access memory (SRAM), reduced latency dynamic random access memory (RLDRAM), double data rate dynamic random access memory (DDR DRAM), double data rate two dynamic random access memory (DDR-2), double data rate three dynamic random access memory (DDR-3), and fast cycle dynamic random access memory (FCDRAM).

57. (New) The system of claim 55, further comprising:

a third memory store coupled with a third interface, wherein the network processor further comprises an interface controller, coupled with the internal interconnect and further coupled with the third memory store via the third interface.

58. (New) The system of claim 57, wherein the third memory store is selected from a group of memory stores consisting of dynamic random access memory (DRAM), Rambus dynamic random access memory (RDRAM), static random access memory (SRAM), reduced latency dynamic random access memory (RLDRAM), double data rate dynamic random access memory (DDR DRAM), double data rate two dynamic random access memory (DDR-2), double data rate three dynamic random access memory (DDR-3), and fast cycle dynamic random access memory (FCDRAM).

59. (New) The system of claim 57, wherein the third interface comprises a front side bus interface, and the interface controller comprises a front side bus controller, wherein the cache management component and the front side bus controller are integrated.

60. (New) The system of claim 55, wherein the cache management component is configured to maintain a hardware-based cache tag array.